Claims 1-26 are currently rejected under 35 U.S.C 103(a) as unpatentable over Beausang et al. (U.S. Patent No. 5703,789) in view of Crouch et al. (U.S. Patent No. 5,592,493). The Applicants respectfully traverse the rejection on the grounds that Crouch et al is directed to an architecture and a method of logic testing, but does not address logic circuit layout and optimization, and in particular does not address the method of the present invention. In examining Crouch et al. in its entirety, there is no discussion of layout or optimization of layout.

The Examiner states that "Crouch et al teach, in Fig. 14, than in order for the transition to occur at E within a clock domain, a transition must occur at P and all the path establishing values must also occur, but in the previous clock cycle domain to the expected transition (col 12, line 52 to col 13, line 50; Fig. 14). The path traversed point E is identified as critical path that must be met such timing condition". This is inaccurate, as Crouch does not discuss a timing condition that must be met for the path, but rather that *"...the path itself must be conditioned to pass the transition. This is done by fixing the off-path values (e.g., the other inputs to an AND gate other than the one input directly in the path) by tracing back through the logic and placing the correct value in scannable elements (as shown by the logic value 1 cells in scan chain segment 306)."* It is important to note that Crouch explicitly teaches that the path must be conditioned, and in the next sentence, describes how the path is conditioned by setting the logic values of certain scannable elements. Crouch further describes a requirement that certain scan elements be able to hold their value for two sample clock cycles.

The method taught by Crouch for conditioning the path that must be conditioned does not require that scan cells be reordered. The only requirements are that certain scan cells be given certain values, and that certain scan cells be able to hold their value for two sample clock cycles. This is not the same as altering a circuit layout in order to meet a timing constraint. The conditioning method of Crouch is part of a method for testing, and is unrelated to layout optimization

The Examiner has rightly stated that "Crouch et al does not explicitly teach reordering scan cells of the scan chain during layout processes of the IC design, based on the partitioning information, by reordering only scan cells of a same set and not re-ordering scan cells of different sets." However, it must be added that Crouch does not imply reordering of scan cells since Crouch is directed to a scan cell architecture, and does not discuss the processes of layout, optimization and simulation of a logic circuit. In essence, Crouch discusses a final product and its function in its idealized state, but is entirely silent with respect to processes of layout and optimization that may or may not be required to realize the final product.

The Examiner has interpreted the "path" discussed by Crouch as a "critical path". It should be noted that there is only one reference to a "critical path" in Crouch (col. 12, line 47): *"This form of testing is used to determine if specific critical paths in the device are meeting their rated propagation time"*. The discussion of Crouch is limited to testing and does not discuss layout.

As used by Crouch et al., the term "clock cycle domain" refers to a period of time and defines a temporal quantity. This is reinforced in the above paragraph by the use of the adjective "previous" to modify the term "clock cycle domain" at col 13 line 8 and the use of the phrase "...one clock cycle domain earlier..." at col 13 line 10. The only usage of the term "clock domain" at col 13 line 11 is actually a reference to a "clock cycle domain" as can be seen from the context.

As used by Crouch, a "clock domain" is used to refer to a portion of a sequential circuit. When a sequential circuit is partitioned by inserting scan cells per the method of Crouch, clock (cycle) domains are created as a matter of course. Partitioning is not done on the basis of clock (cycle) domains. Clock (cycle) domains as described by Crouch are the result of partitioning and not the basis for partitioning.

Upon examination of the teachings of Beausang and Crouch, it can be seen that Beausang is directed to a method for layout of a logic circuit having a scan chain and Crouch is directed to a test architecture and test method using a scan chain. Although similar terminology is used in the two references, the context and meaning are distinct and there is no suggestion to combine them to be found in either reference as required under MPEP 2143.01. The use of similar words or phrases in two references does not constitute a suggestion to combine when the context and meaning the words and phrases are distinct.

In contrast, the term "clock domain" as used in the present invention and in the art in general refers to a spatial domain, more specifically, a "clock domain" is a region

of a circuit in which the timing behavior is identical or very similar. Clock domain boundaries can be established on the basis of multiple clocks driving different parts of a circuit, or can be set by the presence of buffers, DLLs or PLLs.

Since the "clock domain" in the present invention as claimed is fundamentally different from the "clock cycle domain" or "clock domain" of Crouch et al., the Applicants respectfully submits that the present claimed invention is patentable over the combination of Beausang et al. and Crouch et al. In summary, Applicants assert that Claims 1-26 are now in condition for allowance and earnestly solicits such action by the Examiner.

Since the teachings of Crouch et al are silent with respect to the reordering of scan cells during a layout process, the Applicants respectfully submit that the present claimed invention is patentable over the combination of Beausang et al. and Crouch et al. In summary, Applicants assert that Claims 1-26 are now in condition for allowance and earnestly solicits such action by the Examiner.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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